SY5817 8	3	T/R

1	PIN2	I	Logic input of channel 2
2	NIN2	I	Logic input of channel 2
3	PIN3	I	Logic input of channel 3
4	NIN3	I	Logic input of channel 3
5	PIN4	I	Logic input of channel 4
6	NIN4	I	Logic input of channel 4
7	VDD	-	Positive low voltage power supply (+5V)
8	CLK	I	Positive clock input (up to 200MHz)
9	CLKB	I	Negative clock Input (up to 200MHz)
10	GND	-	Drive power ground (0V)
11	PIN5	I	Logic input of channel 5
12	NIN5	I	Logic input of channel 5
13	PIN6	I	Logic input of channel 6
14	NIN6	I	Logic input of channel 6
15	PIN7	I	Logic input of channel 7
16	NIN7	I	Logic input of channel 7
17	PIN8	I	Logic input of channel 8
18	NIN8	I	Logic input of channel 8
19	CLKIF	I	Control of clock interfaceΣ HiГdifferential CMOSΣ LowГLVDS óрлкм internal pullпup resistorú
20	LVOUT8	O	Low voltage output of channel 8
21	GND	-	Drive power ground (0V)
22	HVOUT8	I/O	High voltage output of channel 8
23	VPP	-	Positive high voltage power supply (0 to +100V)
24	HVOUT7	I/O	High voltage output of channel 7
25	VNN	-	Negative high voltage power supply (0 to -100V)
26	VFN	-	Built-in power supply for N-MOS (N1) gate drive
27	LVOUT7	O	Low voltage output of channel 7
28	LVOUT6	O	Low voltage output of channel 6
29	VFP	-	Built-in power supply for P-MOS (P1) gate drive
30	VPP	-	Positive high voltage power supply (0 to +100V)
31	HVOUT6	I/O	High voltage output of channel 6
32	VNN	-	Negative high voltage power supply (0 to -100V)

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33	HVOUT5	I/O	High voltage output of channel 5
34	GND	-	Drive power ground (0V)
35	LVOUT5	O	Low voltage output of channel 5
36	GND	-	Drive power ground (0V)
37	GND	-	Drive power ground (0V)
38	EN	I	Control of drive output enable£ Hiґoff£ Lowґon óрлкм internal pullπup resistorú
39	VSS	-	Negative low voltage power supply (-5V)
40	VLL	-	Positive voltage supply of logic input interface (1.8 to 5V)
41	THP	O	Thermal protection output flag, open N-MOS drain
42	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time óрлкм internal pullπdown resistorú
43	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time óрлкм internal pullπdown resistorú
44	CC0	I	Lower bit of control of PмкNм drive current óрлкм internal pullπup resistorú
45	CC1	I	Upper bit of control of PмкNм drive current óрлкм internal pullπup resistorú
46	LVOUT4	O	Low voltage output of channel 4
47	GND	-	Drive power ground (0V)
48	HVOUT4	I/O	High voltage output of channel 4
49	VNN	-	Negative high voltage power supply (0 to -100V)
50	HVOUT3	I/O	High voltage output of channel 3
51	VPP	-	Positive high voltage power supply (0 to +100V)
52	VFP	-	Built-in power supply for P-MOS (P1) gate drive
53	LVOUT3	O	Low voltage output of channel 3
54	LVOUT2	O	Low voltage output of channel 2
55	VFN	-	Built-in power supply for N-MOS (N1) gate drive
56	VNN	-	Negative high voltage power supply (0 to -100V)
57	HVOUT2	I/O	High voltage output of channel 2
58	VPP	-	Positive high voltage power supply (0 to +100V)
59	HVOUT 1	I/O	High voltage output of channel 1
60	GND	-	Drive power ground (0V)
61	LVOUT 1	O	Low voltage output of channel 1
62	CLKEN	I	Control of clock enable£ Hiґclock disable£ Lowґclock enable óрлкм internal pullπup resistorú
63	PIN 1	I	Logic input of channel 1
64	NIN 1	I	Logic input of channel 1

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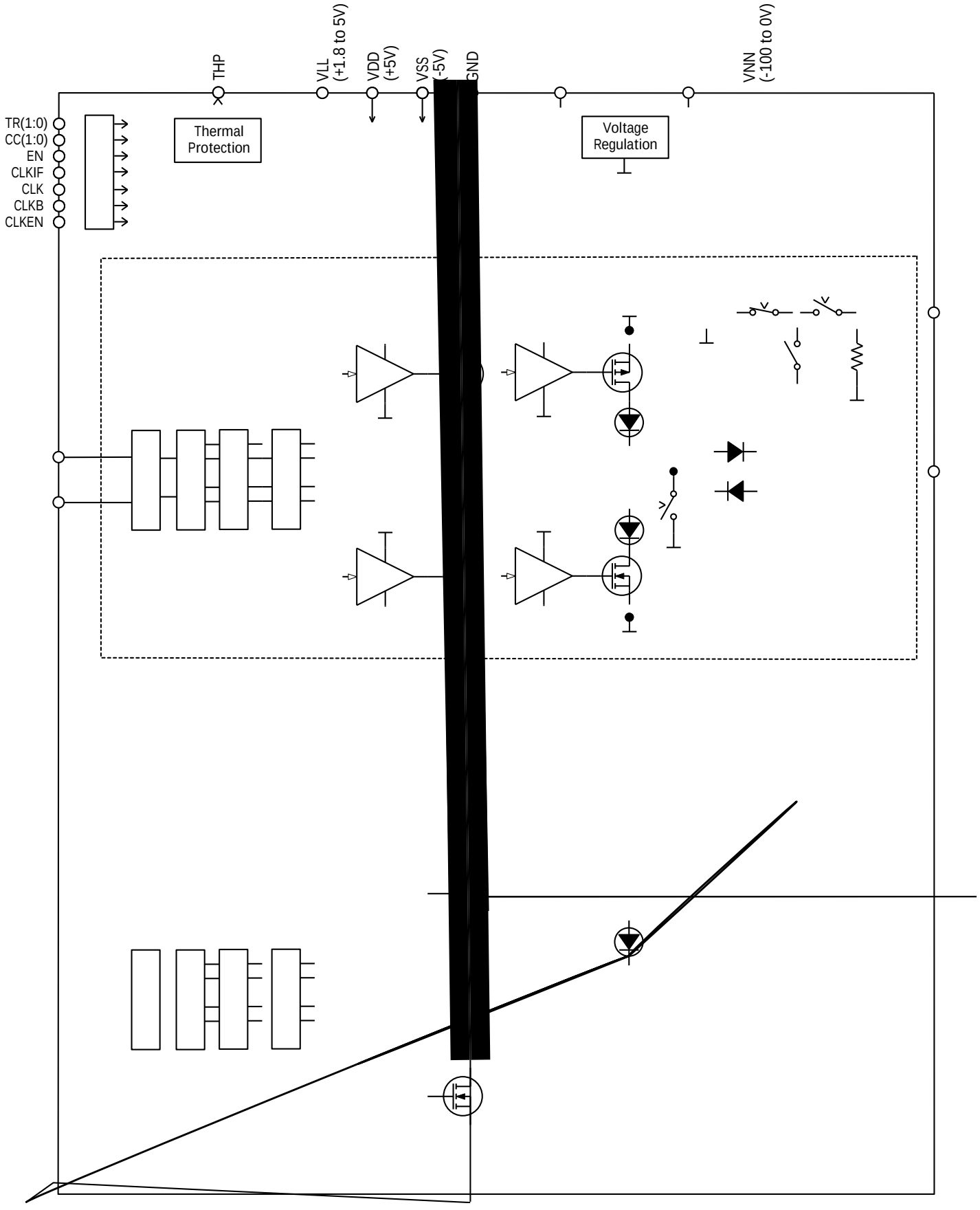
THP
VLL (+1.8 to 5V)
VDD (+5V)
VSS (-5V)
GND
VNN (-100 to 0V)
TR(1:0)
CC(1:0)
EN
CLKIF
CLK
CLKB
CLKEN
Thermal Protection
Voltage Regulation

Fig.1

1,

T_A=25 , unless otherwise specified

Substrate (VSUB, connect to GND) 0V
All Logic I/O and CLK Pins (PINX, NINX, EN, CLKEN, CLK,CLKB, CLKIF, CC(1:0), TR(1:0)) ..... -

Electrical Specifications:V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25 , unless otherwise specified.

V_{LL} current		I_{LLQD}					Quiescent current-1 EN=1(Disable) PINx=NINx=0 Current mode o óCCûмУлбЃ'ûммûÙ V_{PP}/V_{NN}=+/-100V
V_{DD} current		I_{DDQD}					
V_{SS} current							
V_{PP} current							
V_{NN} current							
V_{LL} current		I_{LLQE}					Quiescent current-2 EN=0(Enable) PINx=NINx=0 Current mode o óCCûмУлбЃ'ûммûÙ V_{PP}/V_{NN}=+/-100V
V_{DD} current		I_{DDQE}					
V_{SS} current							
V_{PP} current							
V_{NN} current							
V_{LL} current		I_{LLPW}					PW operating current EN=0 Current mode o óCCûмУлбЃ'ûммûÙ 8-channel active Bipolar 3-level 2-cycle fЃ'pMHÎΣ PRTЃ'нлл>s V_{PP}/V_{NN}=+/-60V
V_{DD} current		I_{DDPW}					
V_{SS} current							
V_{PP} current							
V_{NN} current							
V_{LL} current		I_{LLCW3}					CW operating current-1 EN=0 Current mode o óCCûмУлбЃ'ûммûÙ уπchannel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
V_{DD} current		I_{DDCW3}					
V_{SS} current							
V_{PP} current							
V_{NN} current							
V_{LL} current		I_{LLCW2}					CW operating current-2 EN=0 Current mode н óCCûмУлбЃ'ûмлûÙ уπchannel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
V_{DD} current		I_{DDCW2}					
V_{SS} current							
V_{PP} current							
V_{NN} current							

Electrical Specifications:VLL=2.5V, VDD/VSS=+/-5V, VPP/VNN=+/-60V, TA=25 , unless otherwise specified.

VLL current	TP	ILLCW1	-	0.48	-	mA	CW operating current-3 EN=0 Current mode м óCCώмЎлбГ'ЏлмЏй уπchannel active Bipolar 3-level Continuous f=5MHz VPP/VNN=+/-5V
	LVDS CLK		-	0.58	-	mA	
	CMOS CLK		-	0.53	-	mA	
VDD current	TP	IDDCW1	-	34	-	mA	
	LVDS CLK		-	56	-	mA	
	CMOS CLK		-	53	-	mA	
VSS current		ISSCW1	-	18	-	mA	
VPP current		IPPCW1	-	195	-	mA	
VNN current		INNCW1	-	198	-	mA	
VLL current	TP	ILLCW0	-	0.53	-	mA	CW operating current-4 EN=0 Current mode л óCCώмЎлбГ'ЏллЏй уπchannel active Bipolar 3-level Continuous f=5MHz VPP/VNN=+/-5V
	LVDS CLK		-	0.63	-	mA	
	CMOS CLK		-	0.58	-	mA	
VDD current	TP	IDDCW0	-	28	-	mA	
	LVDS CLK		-	49	-	mA	
	CMOS CLK		-	47	-	mA	
VSS current		ISSCW0	-	13	-	mA	
VPP current		IPPCW0	-	169	-	mA	
VNN current		INNCW0	-	173	-	mA	
LVOUTX output voltage range		LVOUTX	-0.85	-	.+0.85	V	
TRSW on-resistance		ROUTR	-	15	-	м	HVOUTX=100mV, LVOUTX=0V
TRSW on-capacitance		COUTR	-	12	-	pF	LVOUTX=0V
TRSW off-resistance on HVOUTX		ROFFTRHV	1	-	-	Мм	
TRSW off-resistance on LVOUTX		ROFFTRLV	8	10	12	км	
Spike voltage on LVOUTX and LVOUTX		VTRN	-	-	50	mVPP	рлрFккнллм load on HVOUTX нлрFккнллм load on LVOUTX
TRSW turn-on time	TRώмЎлбГ'ЏллЏ	tdTRON	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.6
	TRώмЎлбГ'ЏлмЏ		-	400	-	ns	
	TRώмЎлбГ'ЏмлЏ		-	500	-	ns	
	TRώмЎлбГ'ЏммЏ		-	600	-	ns	
TRSW turn-off time		tdTROFF	-	50	100	ns	See Fig.6
Tx setup time		tTXSU	100	-	-	ns	PINX=NINX=0 (GND) for at least 100ns before Tx burst. See Fig.6
ASW on-resistance		RONASW	-	250	-	м	
Forward voltage		VFHVD	-	1.0	-	V	IF=100mA
			-	1.2	-	V	IF=200mA
Reverse voltage		VRHVD	200	-	-	V	IR=1uA
Forward voltage		VFLVD	-	1.00	-	V	IF=100mA
			-	1.25	-	V	IF=200mA

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Electrical Specifications: V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25 , unless otherwise specified.

Output frequency		f_{OUT}	-	20.0	-	MHz	
Output rise propagation delay	TP mode	t_{dr}	-	31.0	-	ns	See Fig.4
	CLK mode		-	37.0	-	ns	
Output fall propagation delay	TP mode	t_{df}	-	31.0	-	ns	
	CLK mode		-	37.0	-	ns	
Output rise propagation delay clamp	TP mode	t_{drCL}	-	31.0	-	ns	
	CLK mode		-	37.0	-	ns	
Output fall propagation delay clamp	TP mode	t_{dfCL}	-	31.0	-	ns	
	CLK mode		-	37.0	-	ns	
Propagation delay matching		Δt_d	-	±1	±3	ns	
Output rise time		t_r	-	16	-	ns	CC\u0301M\u0301л6Г\u0306мм
			-	24	-	ns	CC\u0301M\u0301л6Г\u0306мл
			-	34	-	ns	CC\u0301M\u0301л6Г\u0306лм
			-	44	-	ns	CC\u0301M\u0301л6Г\u0306лл
		t_{rCL}	-	25	-	ns	See Fig.4
Output fall time		t_f	-	16	-	ns	CC\u0301M\u0301л6Г\u0306мм
			-	24	-	ns	CC\u0301M\u0301л6Г\u0306мл
			-	34	-	ns	CC\u0301M\u0301л6Г\u0306лм
			-	44	-	ns	CC\u0301M\u0301л6Г\u0306лл
		t_{fCL}	-	25	-	ns	
2nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f_{OUT}=5MHz
Pulse cancellation		HDPC	-	-40	-	dBc	
		HDPC2	-	-40	-	dBc	
RMS output jitter		t_J	-	10	-	ps	Bipolar CW, f_{OUT}=5MHz V_{PP}/V_{NN}=+/-5V
Crosstalk between channels		X_{TLK}	-	-70	-	dB	f_{OUT}=5MHz, 10Vp-p HV_{OUT} load Г\u0306рлм
Output enable time	TP	t_{EN}	-	31	-	ns	See Fig.5
	LVDS CLK		-	120	-	ns	
	CMOS CLK		-	140	-	ns	
Output disable time		t_{DS}	-	37	-	ns	
Clock mode enable time		t_{CLKEN}	-	37	-	ns	
Clock mode disable time		t_{CLKDS}	-	37	-	ns	

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Clock (CLK) mode synchronizes data inputs PINX, NINX (X=1~8) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

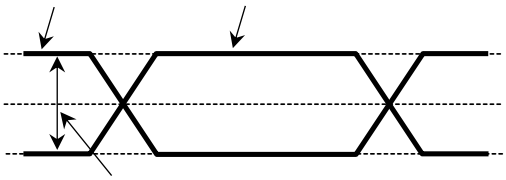
Set CLKEN=0. PINX and NINX are decoded, clocked, level-translated, then sent to high

Table 4 LVDS Clock Inputs (CLK, CLKB)

							20% to 80% of V_{DIFF}

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range (V_{DIFF}(range)



Differential input voltage peak to peak swing (V_{DIFF}(p-p)

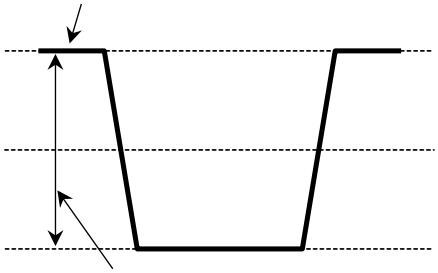


Fig.2 LVDS clock inputs

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.
When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outputs will be enabled.

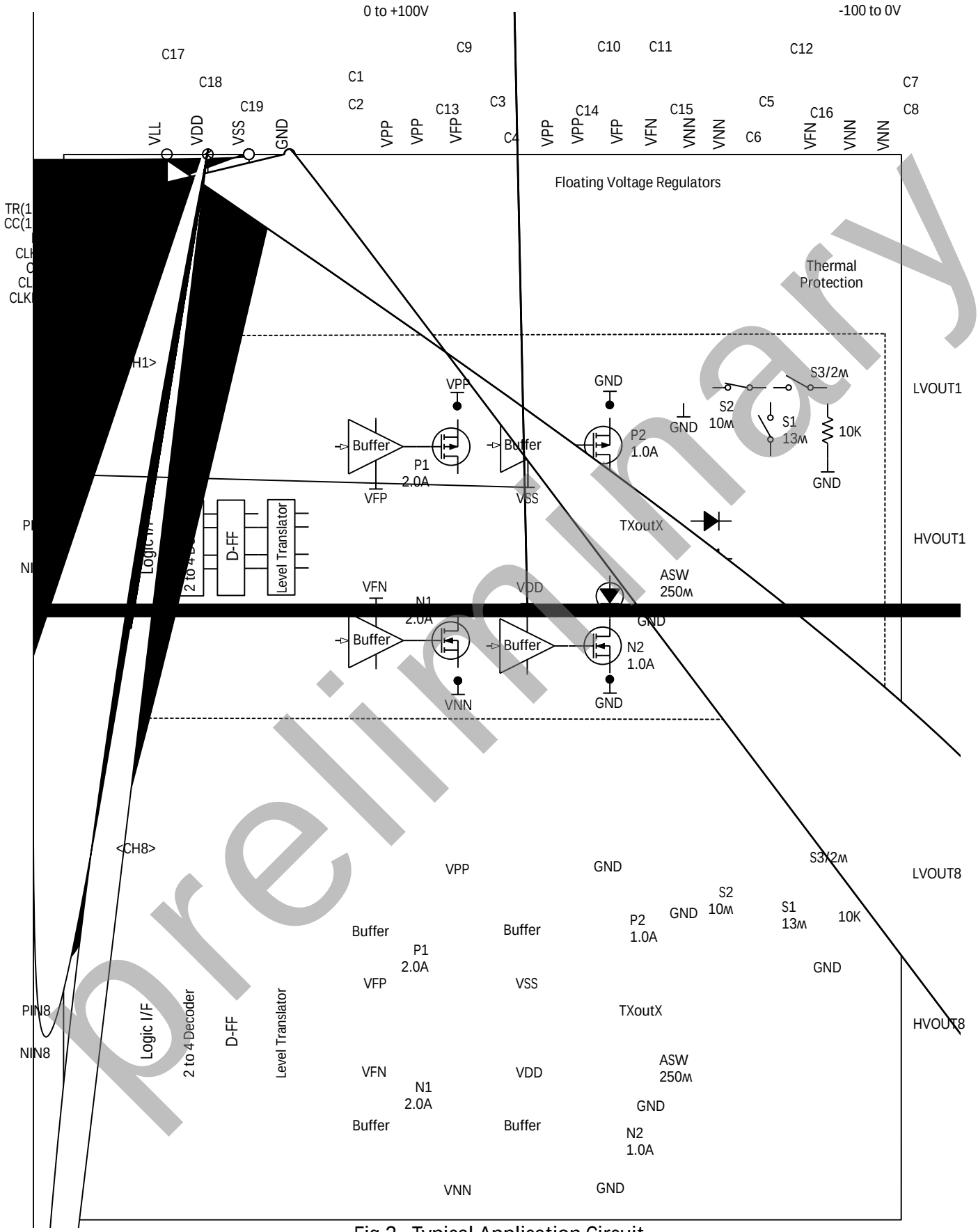


Fig.3 Typical Application Circuit

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Table 6 Static Characteristics

(VDD=5V, TA=25℃ unless otherwise specified)

No.	Items	Symbol	Spec			Units	Conditions
2	HVOUTX high-side peak current	IOH					
4	HVOUTX low-side peak current	IOL					
6	HVOUTX high-side on-resistance	RONH					
8	HVOUTX low-side on-resistance	RONL					

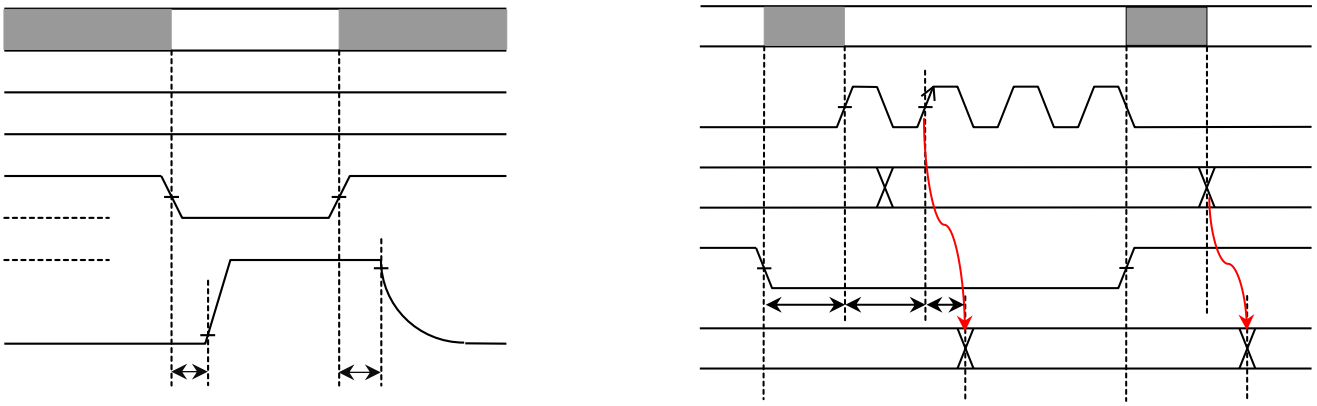


Fig.5 Output enable/disable and Clock enable/disable time

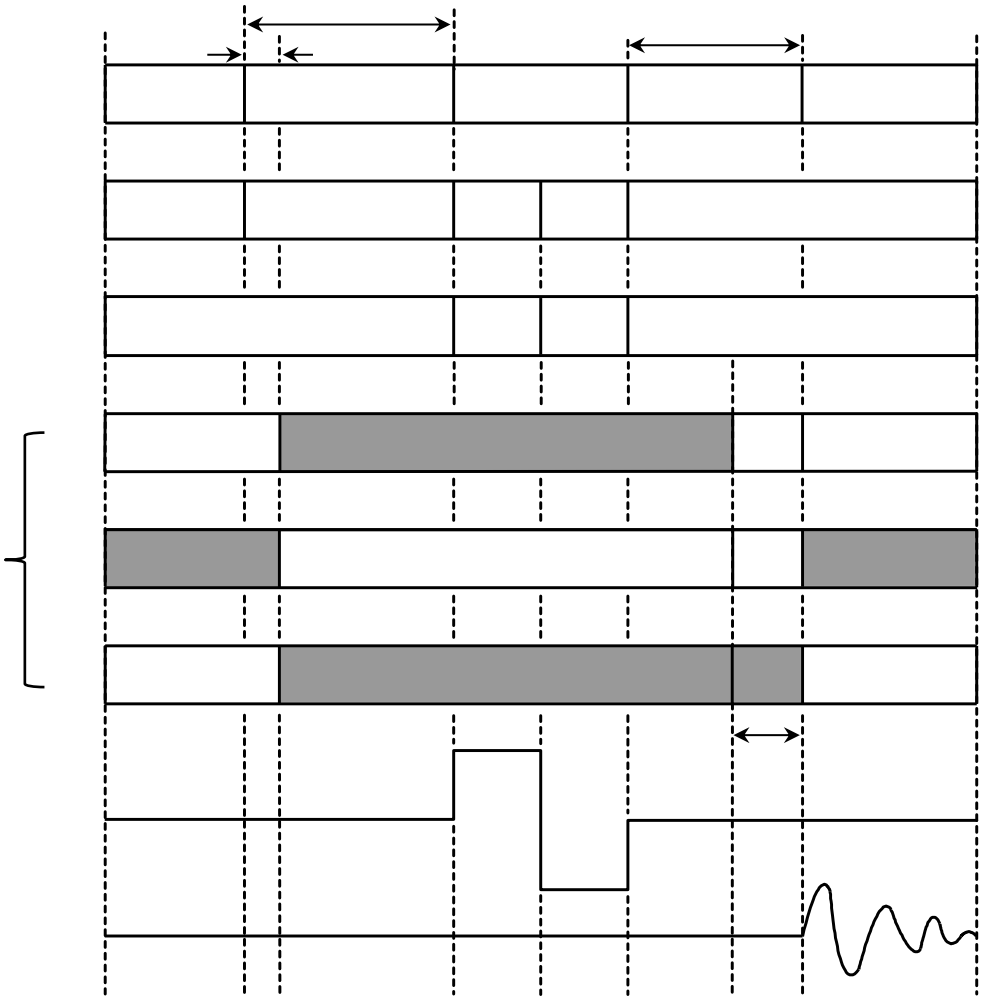


Fig.6 T/R Switch turn-on/off time

Table 13 Truth table

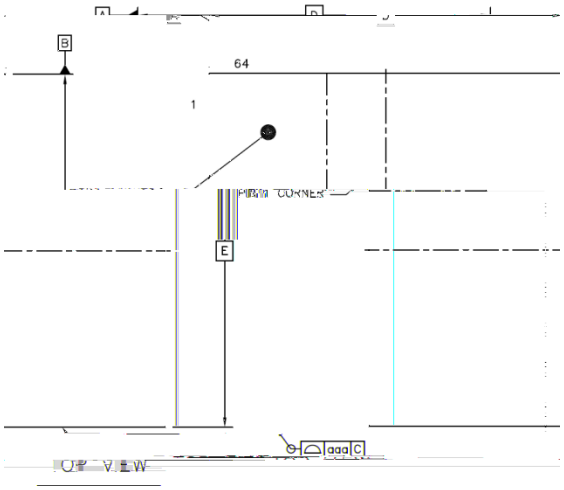
Note: V_{PP}/V_{NN}=+/-HV, x=1~8

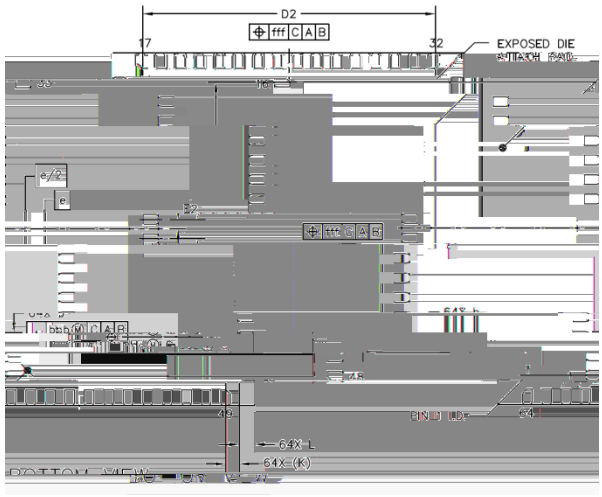
Table 14 P1/N1 drive current mode

Table 15 TRSW S1-S2 turn-on overlap time control mode

Note: Detailed switching time diagram is shown in Fig.6.

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch





Notes:

LLLLLLL
YYWW
SY5817

L = Lot Number
YY = Year Sealed
WW = Week Sealed

64-Lead QFN

PART NO. XX XX

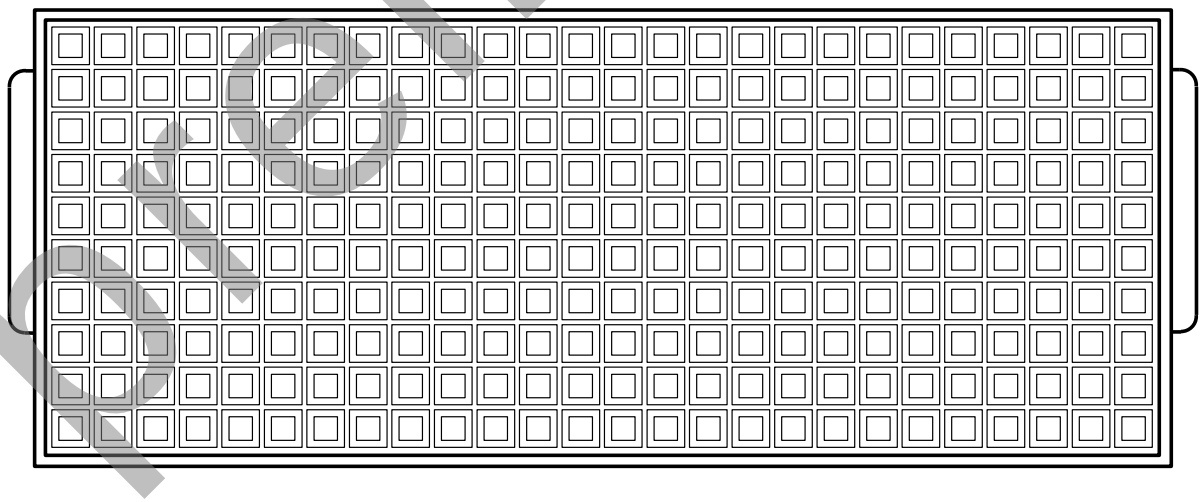
Device Package Media Type

Device: SY5817: 8-Channel 3-Level HV Ultrasound Transmitter with T/R switch

Package: FN: QFN

Media Type: (blank): 2600pcs for MOQ

SY5817FN: 8-Channel 3-Level HV Ultrasound Transmitter with T/R switch
64-lead QFN, 9.00x9.00mm
260/Tray x10 for MOQ



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Rev 0.0	2025-05-08		Initially released as preliminary specification

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