32

- CMOS SY2320 32
-
- 32
- 3.3V
-

SY2320

	64-Lead LGA 9.00x9.00mm body 0. mm !"#$!% 0.50mm p#%&!
SY2320	SY2320' (

Parameter	Value
V_{DD} logic supply	-0.5V to +7.0V
V_{PP}-V_{NN} differential supply	140V
V_{PP} positive supply	-0.5V to V_{NN}+140V
V_{NN} negative supply	+0.5V to -70V
Logic input voltage	-0.5V to V_{DD} +0. V
!nalog signal range	V_{NN} to V_{PP}
Pea" analog signal current#c$annel	'.0!
%torage te&perature	-(5)* to 150)*
Po+er dissipation, (4-Lead L - !	1.5 .

#bsolute $a%imum Ratin&s are those 'alues be(ond whi"h dama&e to the de'i"e ma(o""ur.)un"tional operation under these "onditions is not implied. *ontinuous operation of the de'i"e at the absolute ratin& le'el ma(affe"t de'i"e reliabilit(. #ll 'olta&es are referen"ed to de'i"e &round.

Sym	Parameter	Value
V_{DD}	Logic po+er supply voltage	.0V to 5.5V
V_{PP}	Positive ig voltage supply	+40V to V_{NN} +1'0V
V_{NN}	Negative ig voltage supply	-40V to -(0V
$V_{1/}$	/ig$ level input voltage	0.0V_{DD} to V_{DD}
V_{1L}	Lo+ level input voltage	0V to 0.1V_{DD}
V%1-	!nalog signal voltage pea"-to-pea"	V_{NN}+5V to V -5V PP
2!	3perating free air te&perature	0)* to 70)*

Notes:

1. and powered-down last.
2. V_{SIG} must be within V_{NN} and V_{PP}
3. Rise and fall times of power supplies V , V_{PP}, and V_{NN} should not be less than 1.!mse".

preliminary

DC Electrical Characteristics

+o'er re"ommended operatin& "onditions unless otherwise noted,

Sym	Parameter	0°C		+25°C			+ 0°C		!nits	Con"itions	
		#in	#a$	#in	%yp	#a$	#in	#a$			
53N%	%&all signal s+itc$ 3N-resistance	-	-	-	-	-	-	-	Ω		
		-	-	-	-	-	-	-			
		-	-	-	'5	-	-	-		1%1- 4 5.0& !	V_PP 4 +(0V V_NN 4 -(0V
		-	-	-	17	-	-	-		1%1- 4 '00& !	
		-	-	-	-	-	-	-			
		-	-	-	-	-	-	-			
ΔR3N%	%&all signal s+itc$ 3N-resistance &atc$ing	-	'0	-	5.0	'0	-	'0	7	1%1- 4 5.0& !6 V_PP 4 +(0V6 V_NN 4 -(0V	
53NL	Large signal s+itc$ 3N-resistance	-	-	-	5	-	-	-	Ω	V%1- 4 VPP -10V6 1%1- 4 1.0 !	
5IN2	Value of output 8leed resistor	-	-	'0	5	50	-	-	kΩ	3utput %+itc$ to 5 - ND 15IN2 4 0.5& !	
1%3L	%+itc$ 3 : : lea"age per s+itc$;	-	5.0	-	1.0	10	-	15	9!	V%1- 4 VPP -5V and VNN +5V	
V3%	D* offset s+itc$ 3 : : ;	-	00	-	100	00	-	00	&V	No Load	
	D* offset s+itc$ 3N;	-	500	-	100	500	-	500	&V		
1PP=	=uiescent VPP supply current	-	-	-	'.<	-	-	-	9!	!ll s+itc$es 3 : :	
1NN=	=uiescent VNN supply current	-	-	-	-.1	-	-	-	9!	!ll s+itc$es 3 : :	
1PP=	=uiescent VPP supply current	-	-	-	'.(	-	-	-	9!	!ll s+itc$es 3N6 1%. 4 5.0& !	
1NN=	=uiescent VNN supply current	-	-	-	-.0	-	-	-		!ll s+itc$es 3N6 1%. 5.0&	
1%.	%+itc$ output pea" current	-	'.0	-	-	'.0	-	'.0	!	V%1- duty cycle ? 0.1 7	
f%.	3utput s+itc$ing fre>uency	-	-	-	-	50	-	-	"/@	Duty cycle 4 50 7	
1PP	!verage VPP supply current	-	-	-	-	-	-	-	&!	V_PP 4 +(0V V_NN 4 -(0V	!ll output s+itc$es are turning 3N and 3 : : at 50"/@ +it$ no load.
		-	0.5	-	-	0.(	-	-			
		-	-	-	-	-	-	-			
1NN	!verage VNN supply current	-	-	-	-	-	-	-	&!	V_PP 4 +(0V V_NN 4 -(0V	!ll output s+itc$es are turning 3N and 3 : : at 50"/@ +it$ no load.
		-	0.0	-	-	1.1	-	-			
		-	-	-	-	-	-	-			
1DD	!verage VDD supply current	-	0.5	-	-	0.(	-	-	&!	f*LA 4 5.0B/@6 VDD 4 10.0V	
1DD=	=uiescent VDD supply current	-	45	-	-	50	-	-	9!	!ll logic inputs are static	
1%35	Data out source current	0.45	-	0.45	0.70	-	0.40	-	&!	V3c2 4 VDD - 0.7V	
1%INA	Data out sin" current	0.45	-	0.45	0.70	-	0.40	-	&!	V3c2 4 0.7V	
*IN	Logic input capacitance	-	10	-	-	10	-	10	p:	---	

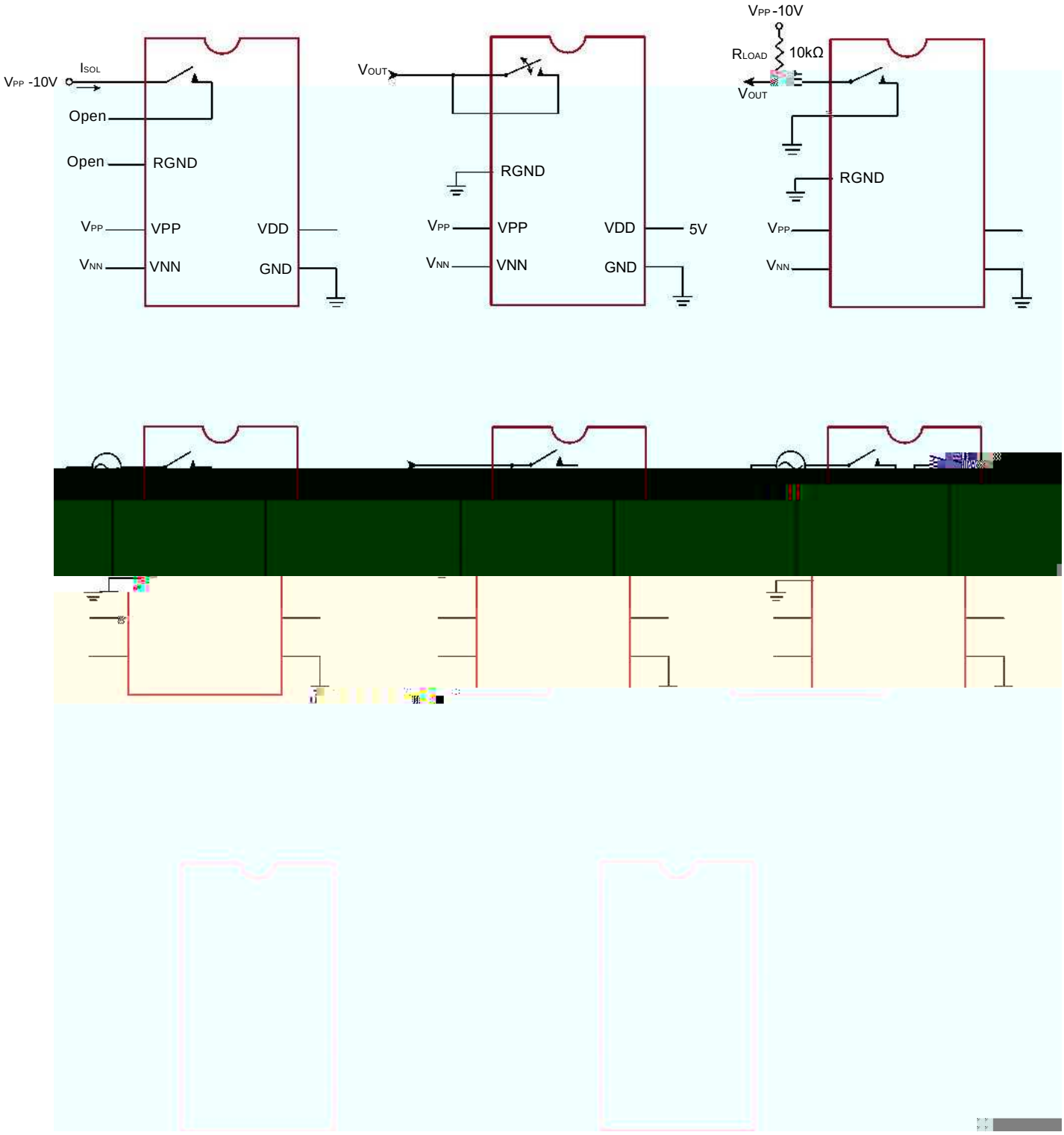
preliminary

&C Electrical Characteristics

+o'er re"ommended operatin& "onditions, V - ..!V, t_R - $t_)$

Sym	Parameter	0°C		+25°C			+ 0°C		!nits	Con"itions
		#in	#a$	#in	%yp	#a$	#in	#a$		
$t_{\%D}$	%et up ti&e 8efore $\overline{LD}$ rises	'5	-	'5	-	-	'5	-	ns	---
t.LD	2i&e +idt$ of $\overline{LD}$	5(	-	-	5(	-	5(	-	ns	V_{DD}4 .0V
		1'	-	-	1'	-	1'	-		V_{DD}4 5.0V
t_{D3}		50	100	50	7<	100	50	100		V_{DD}4 .0V
		15	40	15	0	40	15	40		
t.*L5		55	-	55	-	-	55	-		
$t_{\%C}$		'1		-			'1			
		7.0					7.0			
		'.0					'.0			
		-					-			

SY2320 Test Circuits



Pin Function

Pin	Function
1	SW30
2	Y3031
3	SW31
4	NC
5	CLR
6	NC
7	$\overline{LE}$

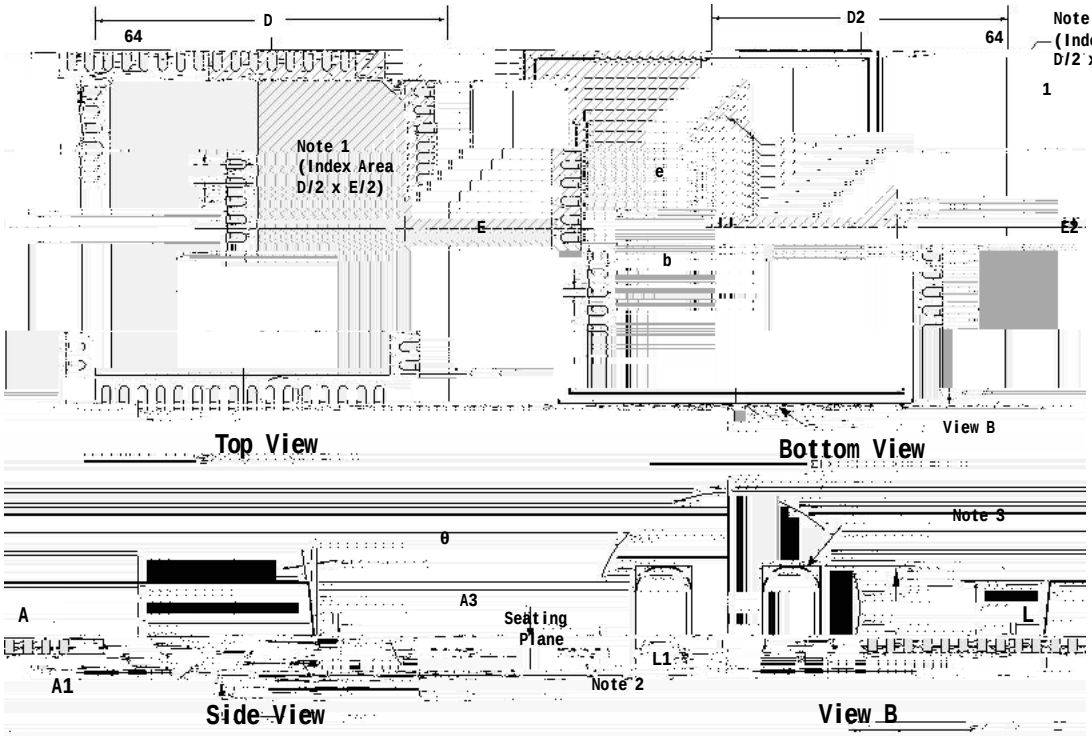
Pin	Function
17	SW2
18	Y23
19	SW3
20	SW4
21	Y45
22	SW5
23	SW6
24	Y67
25	
26	
27	
28	
29	
30	
31	
32	

Pin	Function
33	Y1213
34	SW13
35	VPP
36	RGND
37	VNN
38	SW14
39	Y1415
40	SW15
41	SW16
42	Y1617
43	SW17
44	VNN
45	
46	
47	
48	

Pin	Function
49	SW19
50	SW20
51	Y2021
52	SW21
53	SW22
54	Y2223
55	SW23
56	SW24
57	Y2425
58	SW25
59	SW26
60	Y2627
61	SW27
62	SW28
63	Y2829
64	SW29

64-Lead LGA Package Outline

9.00x9.00mm body, 0.75mm height (max), 0.50mm pitch



Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.65	0.00	0.20 REF	0.20	8.90	7.60	8.90	7.60	0.50 BSC	0.30	0.00	0 °
	NOM	0.70	0.02		0.25	9.00	7.70	9.00	7.70		0.40	-	-
	MAX	0.75	0.05		0.30	9.10	7.80	9.10	7.80		0.50	0.15	14 °